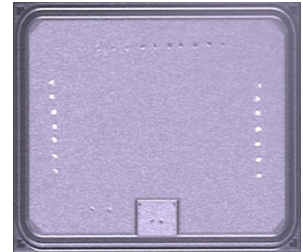


## Field Stop IGBT Chip

# FGA60N65SM

**650V, 60A,  $V_{CE(sat)} = 1.9V$**

Part	$V_{CES}$	$I_{Cn}$	$V_{CE(sat)}$ Typ	Die Size
FGA60N65SM	650V	60A	1.9	6.3 x 5.7 mm <sup>2</sup>
See page 2 for ordering part numbers & supply formats				



### Applications

- Inverter Modules
- Welding & Drive Applications

### Features

- Low Saturation Voltage
- Fast Switching:  $E_{OFF} = 7.5\mu\text{J/A}$
- Tightened Parameter Distribution

### Maximum Ratings

Symbol	Parameter	Ratings	Units	
$V_{CES}$	Collector to Emitter Voltage	650	V	
$V_{GES}$	Gate to Emitter Voltage	$\pm 20$	V	
$I_C$	Collector Current <sup>1</sup>	Continuous ( $T_C = 25^\circ\text{C}$ )	120	A
		Continuous ( $T_C = 100^\circ\text{C}$ )	60	A
$I_{CM}$	Pulsed Collector Current	180	A	
$T_J, T_{STG}$	Operation Junction & Storage Temperature	-55 to 175	$^\circ\text{C}$	

### Static Characteristics, $T_J = 25^\circ$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{CES}$	Collector to Emitter Breakdown Voltage	$V_{GE} = 0V, I_C = 250\mu\text{A}$	650	-	-	V
$I_{CES}$	Collector Cut-Off Current	$V_{CE} = V_{CES}, V_{GE} = 0V$	-	-	250	$\mu\text{A}$
$I_{GES}$	G-E Leakage Current	$V_{GE} = V_{GES}, V_{CE} = 0V$	-	-	$\pm 400$	nA

### On Characteristics, $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GE(th)}$	G-E Threshold Voltage	$I_C = 250\mu\text{A}, V_{CE} = V_{GE}$	3.5	4.5	6.0	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	$I_C = 60A, V_{GE} = 15V$	-	1.9	2.5	V
		$I_C = 60A, V_{GE} = 15V$ $T_C = 175^\circ\text{C}$	-	2.1	-	V

## Dynamic Characteristics<sup>2</sup>, T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C <sub>ies</sub>	Input Capacitance	V <sub>CE</sub> = 30V, V <sub>GE</sub> = 0V f = 1MHz	-	2915	-	pF
C <sub>oes</sub>	Output Capacitance		-	270	-	
C <sub>res</sub>	Reverse Transfer Capacitance		-	85	-	
Q <sub>g</sub>	Total Gate Charge	V <sub>CE</sub> = 400V, I <sub>C</sub> = 60A V <sub>GE</sub> = 15V	-	189	-	nC
Q <sub>ge</sub>	Gate to Emitter Charge		-	20	-	
Q <sub>gc</sub>	Gate to Collector Charge		-	91	-	

## Switching Characteristics<sup>3</sup>, T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>CC</sub> = 400V, I <sub>C</sub> = 60A R <sub>G</sub> = 3Ω, V <sub>GE</sub> = 15V Inductive Load, T <sub>C</sub> = 25°C	-	18	-	ns
t <sub>r</sub>	Rise Time		-	47	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	104	-	ns
t <sub>f</sub>	Fall Time		-	50	-	ns
E <sub>on</sub>	Turn-On Switching Loss		-	1.54	-	mJ
E <sub>off</sub>	Turn-Off Switching Loss		-	0.45	-	mJ
E <sub>ts</sub>	Total Switching Loss		-	1.99	-	mJ
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>CC</sub> = 400V, I <sub>C</sub> = 60A R <sub>G</sub> = 3Ω, V <sub>GE</sub> = 15V Inductive Load, T <sub>C</sub> = 175°C	-	18	-	ns
t <sub>r</sub>	Rise Time		-	41	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	115	-	ns
t <sub>f</sub>	Fall Time		-	48	-	ns
E <sub>on</sub>	Turn-On Switching Loss		-	2.08	-	mJ
E <sub>off</sub>	Turn-Off Switching Loss		-	0.78	-	mJ
E <sub>ts</sub>	Total Switching Loss		-	2.86	-	mJ

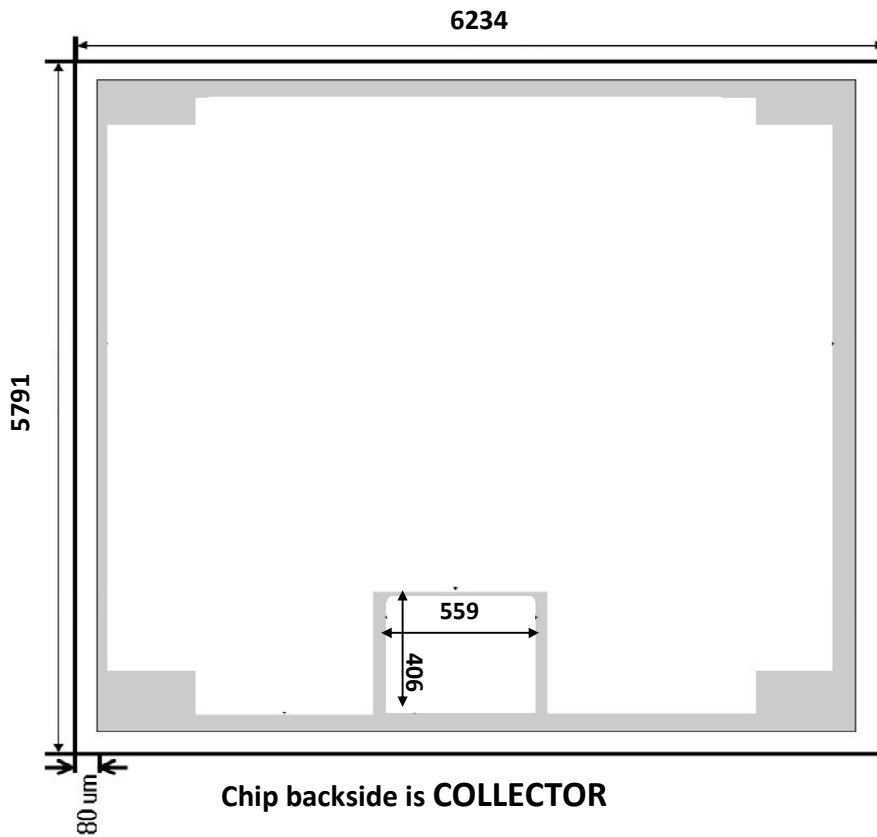
### Notes:

1. Performance will vary based on assembly technique and substrate choice
2. Defined by chip design, not subject to 100% production test at wafer level
3. Specified in discrete package for indicative purposes only, bare die performance will vary depending on module design.

## Ordering Guide

Part Number	Format	Detail / Drawing
FGA60N65SMMW	Un-sawn wafer, electrical rejects inked	Page 3
FGA60N65SMMF	Sawn wafer on film-frame	Page 4
FGA60N65SMMD	Singulated die / chips in waffle pack	Page 4
Note: Singulated Die / Chips can also be supplied in Pocket Tape or SurfTape® on request		

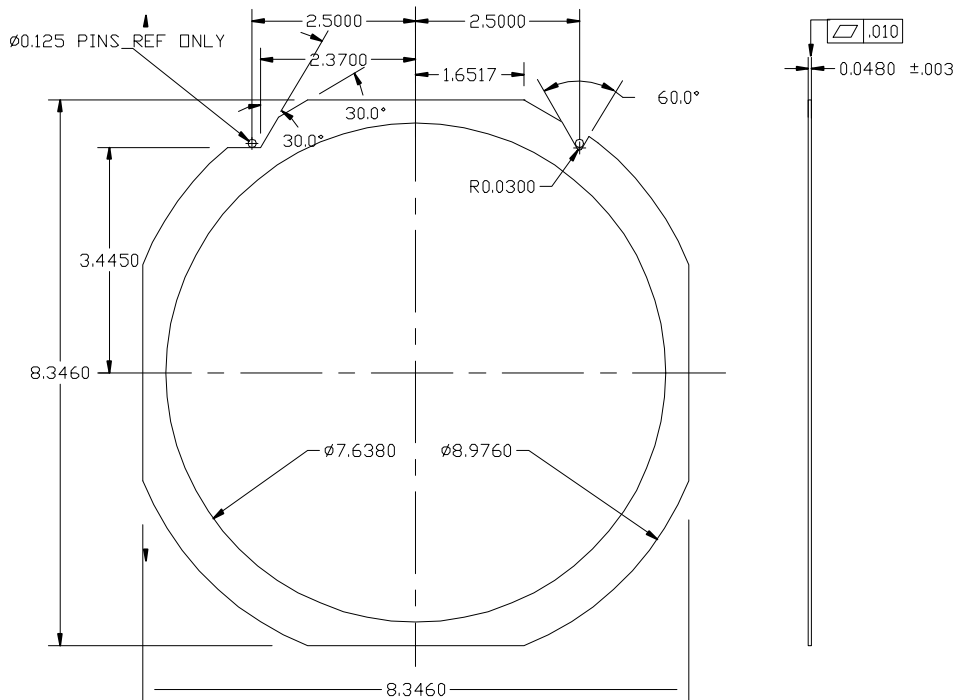
## Die Drawing – Dimensions (µm)



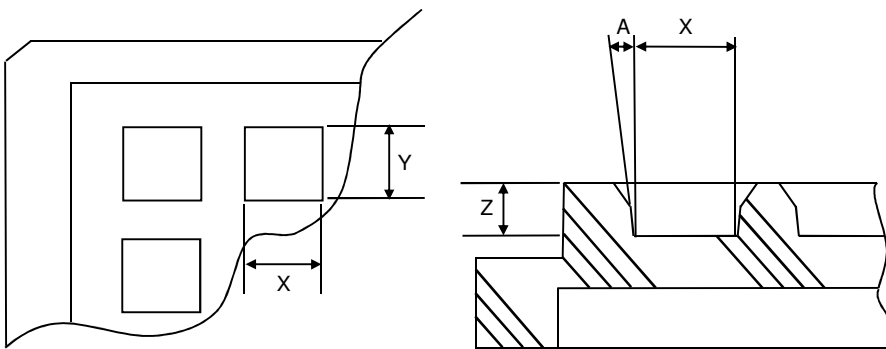
## Mechanical Data

Parameter			Units
Chip Dimensions Un-sawn	6324 x 5791		µm
Chip Thickness (Nominal)	75		µm
Gate Pad Size	559 x 406		µm
Wafer Diameter	150 (subject to change)		mm
Saw Street	80 (subject to change)		µm
Wafer orientation on frame	Wafer notch parallel with frame flat		
Topside Metallisation & Thickness	Al	4	µm
Backside Metallisation & Thickness	V/Ni/Ag	0.45	µm
Topside Passivation	Silicon Nitride		
Recommended Die Attach Material	Soft Solder or Conductive Epoxy		
Recommended Wire Bond - Gate	Al 150µm X1		
Recommended Wire Bond – Source	Al 500µm X2		

## Sawn Wafer on Film-Frame – Dimensions (inches)



## Die in Waffle Pack – Dimensions (mm)



X = 6.6mm  $\pm$ 0.13mm pocket size  
 Y = 6.6mm  $\pm$ 0.13mm pocket size  
 Z = 0.41mm  $\pm$ 0.08mm pocket depth  
 A = 5°  $\pm$ 1/2° pocket draft angle  
 No Cross Slots  
 Array = 6 X 4 (24)

### OVERALL TRAY SIZE

Size = 50.67mm  $\pm$ 0.25mm  
 Height = 3.94mm  $\pm$ 0.13mm  
 Flatness = 0.30mm

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