Micross provides comprehensive semiconductor packaging services for multiple electronic components, including digital, mixed signal, analog, multi-chip and System-in-Package (SiP). We design, build and test hermetic QML and chip scale packaging for various markets including down-hole, aerospace, satellite and military.

We combine advanced processes and product development to provide full turnkey support for prototype to volume production of flip chip and wire bond packages including single chip, multichip and SiP applications on organic substrates or ceramic substrates.

By ensuring delivery of finished wafers through our relationships with silicon OCMs, and full coordination of customer BOM requirements, we offer complete supply-chain management services for micro-electronic assemblies.

Micross supplies modules and contract assembly services for multiple platforms: industrial, airborne; commercial and government satellites; missile and ordnance; C4ISR and medical.

Custom Multichip Packaging (MCP) is a die based system or sub-system assembled into a single package which is then mounted to the PCB. In its simplest form factor, two or more of the same die are combined in one industry standard package that is smaller than the equivalent single die packages combined. This provides the user with density and performance two to three generations ahead of current semiconductor fab processes.

Typically, multichip or system in a package devices are comprised of multiple memory die, but often include a processor, gate array, ASIC, or other logic as demanded by the customers application. They can also be combined with other components such as registers, clocks, sensors, triggers, passives, MEMS, voltage regulators, etc.

Micross serves the defense aerospace, medical, industrial and space markets with these technologies. Design, assembly and test are performed in an on shore MIL-PRF-38535, MIL-PRF-38534 facility certified by DSCC to class V and H.
Facility and Quality

- DSCC QML
  - MIL-PRF-38534, Class H (Class K in process)
  - MIL-PRF-38535, Class Q
  - MIL-PRF-38535, Class V (assembly)
  - Laboratory Suitability (MIL-STD-883)
- SMD, Q and M level
- Certification of wafer traceability lot to Class H or Class K requirements.
- All die preparation, sample assembly, evaluation and test per Table C-II in-house with full traceability and MIL-STD-883 DSCC Laboratory Certification.
- NSTS 5300.4
- Capabilities for Class S manufacturing
- AS9100 Rev. C registered
- Customer specific, Source Control Drawing (SCD)

Packaging Options

- Surface mount
  - Plastic Ball Grid Array (PBGA)
  - Chip Scale Package (CSP)
  - Ceramic and HitCE Ceramic BGA (see Table 1)
  - Ceramic Flat Pack (FP)
  - Ceramic Quad Flat Pack (QFP)
  - Ceramic gull wing
  - Plastic, Small-Outline, J-ledged (CSOJ)
  - SOJ, QFP, and TSOP as open cavity
  - Plastic, Thin Quad Flat Package (TQFP)
  - Ceramic Leadless Chip Carrier (CLCC)

- Through-hole
  - Pin Grid Array (PGA)
  - Ceramic Dual-In-Line Package (CDIP)
  - Zig-Zag in-line (ZIP)
  - Metal can

Services

- Die banking and parts management
- Total turnkey manufacturing, full BOM management
- DMS/obsolescence mitigation
- Die banking and diminished sources (End of Life) support. Micross die bank is equipped with state-of-the-art climate control systems and nitrogen-purged dry boxes. We store and handle inventory per military/industry specifications and provide internal class A and B die inspection.
- Obsolete and legacy products support
- Flexible, personalized customer support

Engineering & Analytical Services

- Scanning Electron Microscopy (SEM)
- Decapsulation
- Demarking and ink or laser mark
- Lot Acceptance Testing
- Design of substrates, plastic/laminate or hermetic ceramic
- Test, burn-in and qualification
- Visual inspection insures defect free die products
- Wafer probe insures post-assembly integrity
- Pick and place automation for quick and precise custom packaging
- Component evaluation and qualification
- Package and sub-assembly design
- Device characterization
- Infant mortality testing
- Sonoscan (CSAM), X-ray
- Stud pull, bond pull
- Moisture resistance
- Steam age/solderability
- Salt spray
- Thermal shock/thermal analysis

Test

- Hot probe to 150°C
  - Can be tooled for full functional test
  - Capacity dependent on complexity of die and die/wafer
- Full temperature upscreening
- Testing for memory, mixed signal, LSI, VLSI, linear, logic, ASICs, RF, and discretes
- Custom test equipment
- Test equipment
  - Agilent 83000
  - Mixed Signal LTX Credence D10
  - Memory test - Teradyne J937
  - Teradyne A585
  - Testronics 201 and FET9400
  - Linear Test Systems LTX TS80
  - ECL test system
  - Delta flex pick & place handlers
  - Symtek handlers - X1 & X4
  - Temptronics temperature forcing systems (-65°C to +150°C capability)
  - Automated Bench Test
- Full static/dynamic burn-in
  - Burn-in boards
  - Convection ovens
  - Static and dynamic Wakefield chambers
  - Class 100 Clean Room
Typical material properties of widely used interposers for multichip packaging

<table>
<thead>
<tr>
<th>Material</th>
<th>TCE</th>
<th>TCE</th>
<th>Thermal Conductivity</th>
<th>Dielectric Constant</th>
<th>Typical Conductor Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>40°C</td>
<td>25°C</td>
<td>125°C</td>
<td>W/mK</td>
<td>1MHz 3.2GHz</td>
</tr>
<tr>
<td>High T_g lamiante (~300)</td>
<td>12-13</td>
<td>14-15</td>
<td>16-17</td>
<td>0.2</td>
<td>4.7</td>
</tr>
<tr>
<td>High TCE ceramic</td>
<td>8-8.5</td>
<td>8.5-9.0</td>
<td>10-11</td>
<td>2.0</td>
<td>9.4 9.5</td>
</tr>
<tr>
<td>Alumina ceramic Al_2O_3</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>18</td>
<td>10</td>
</tr>
</tbody>
</table>

Multichip designs are assembled on an interposer or substrate to create a customized, integrated product for a unique application. Within the multichip package, the designer can utilize bare die (wire bond or flip chip), WLCSP devices or stacked die. The critical benefits of this technology include:

- Greater functionality in a faster time-to-market window than could be done through silicon integration or ASIC development.
- Reduced cost compared to an ASIC.
- Increased density and performance with reduced PCB area utilization; reduced down routing at the PCB level and reduced weight. Reduced down routing can provide potential PCB layer reduction and lower PCB costs.
- Design optimization through use of the most cost effective silicon solutions; assembling various semiconductor technologies, die geometries, or silicon from different fabs in the same multichip package.
- Improved signal integrity from reduced trace lengths.
- Reduced PCB assembly complexity and wider pitches, leading to simplified Class 3 PCB compliance.
- Allows the OEM to upgrade products, meet tech refreshes, or pre-planned product improvements, by using die shrinks in the same package.
- Depending on environmental requirements, the MCP can be in a ceramic hermetic or plastic encapsulated packages.
Robotic Hot Solder Dipping & Solder Exchange

**Micross SXT™** (Solder Exchange Technology) is a robotic, automated solder-dipping process developed by Micross Components to increase component reliability and mitigate tin-whisker formation. With **Micross SXT™**, unwanted finish can be replaced on a wide range of electronic components regardless of packaging style.

The GEIA-STD-0006 compliant process includes:

- Robotic-controlled six-axis dipping
- Solder dipping under a nitrogen blanket
- Solder-level sensing for accurate solder dipping
- Integral component wash and dry facility
- Preheating of components to negate thermal shock
- Lead tinning/solder dip
- Terminal finish conversion
- Solder exchange from Pb free (RoHS) ↔ SnPb

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### Hi-Rel Lead Attach

- Thermocompression weld lead and high-temp solder lead attachment processes
- J, Gullwing, and Spider Gullwing lead forms

### Trim & Form Components

- Trim, form, and solder dip to SOIC, SOJ packages (other packages not limited to DIP, PSOP, TSOP, FP's and QFP's)
- Realign and Reform Component Leads

### BGA Modifications

- BGA re-balling for conversion to tin-lead (SnPb)
- Ball attach
- BGA re-work

### Test

- X-ray fluorescence analysis (XRF)
- Ionic cleanliness test
- Solderability testing
- Particle Impact Noise Detection test (PIND)
- Fine and gross leak testing
- Lead integrity/bond strength

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Anti-Counterfeit Program & BOM Management

Micross Components is uniquely positioned to take a trusted role in your semiconductor supply chain to provide a counterfeit-free purchasing experience. Throughout our 35+ year history of providing authentic high-reliability products, we’ve developed the software and the skills needed to handle everything from diodes to microprocessors.

If counterfeit protection is what you’re looking for... **Get Real. Get Micross.**