Quality - by Design

Quality
Design Review
Stages

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Design Review Stages

- Design Review 0 (DR0)
  - Pre-order & quotation stage
- Design Review 1 (DR1)
  - Initial kick-off and preliminary specification review
- Design Review 2 (DR2)
  - Pre-layout simulation review of final design
- Design Review 3 (DR3)
  - Post-layout simulation review of final design
  - Layout DRC, ERC & LVS review
- Design Review 4 (DR4)
  - Prototype review
- Design Review 5 (DR5)
  - Production review
Design Review 0

DR0

- Design
  - Target Specification, description & schematics etc.,
- Planning
  - Development plan, proposed sample & production timescales.
  - Production quantities.
- Manufacturing
  - Package type & general specification.
  - Tester & tooling requirements.
- Commercial
  - Unit cost estimates, volumes, ASP, & NRE costs.
  - Special costs (Tooling, qualification).
- Safety & Reliability
  - Design safety & reliability requirements.
  - Product life-cycle requirements.
  - Environmental conditions.
  - Qualification requirements.
From **DR0** to **DR1**

1. DR0 Customer Contact
2. Draft Specification
3. Feasability & Technology Studies
4. Quotation
5. DR1 Customer Review
Design Review 1

DR1

• Design
  – Target Specification, description & schematics etc.,
  – Wafer fab technologies, design rules, special issues

• Planning
  – Task allocation & resources
  – Development plan, sample & production timescales
  – Production quantities & schedules

• Manufacturing
  – Package type, package approval status & general specification
  – Tester, tooling & assembly requirements

• Commercial
  – Die size estimates, unit cost estimates, wafer costs & yields
  – Capital & Tooling costs

• Quality, Safety, Reliability & Risk assessment.
  – Quality plan
  – Risks - Identification & Assessment
  – Design safety & reliability requirements, with life-cycle definition.
From **DR1** to **DR2**

- DR1 Customer Review
- Schematic Capture
- VHDL Text
- Synthesis
- Netlist & Simulation
- DR2 Acceptance
Design Review 2

- **Design**
  - Specification, description, block diagrams & schematics etc.,
  - Simulation data.
  - Performance against specification, any special issues.
- **Planning**
  - Progress and outstanding actions.
  - Development plan, with sample timescales.
  - Production quantities & schedules.
- **Manufacturing**
  - Package type, package approval status & general specification.
  - Assembly requirements, piece parts & travellers.
- **Commercial**
  - Die size estimates, unit cost estimates, wafer costs & yields, any changes ?
- **Quality, Safety, Reliability & Risk assessment.**
  - Quality plan review & update
  - Risks - review, any new risks identified ?.
From **DR2 to DR3**

- **DR2 Acceptance**
- **Manual Layout**
- **Auto Place & Route**
- **DRC / ERC / LVS & Extraction**
- **Post-Layout Simulation & Chip Finish**
- **DR3 Acceptance**
Design Review 3

**DR3**

- **Design**
  - Specification, description, block diagrams & schematics etc.,
  - Layout and post-Layout Simulation data, performance issues.
  - LVS, DRC, ERC, Customer checks, die fiducials, Bonding data.

- **Planning**
  - Progress and outstanding actions.
  - Update of development plan, with sample timescales.
  - Update of Production quantities & schedules.

- **Manufacturing**
  - Bonding diagram, branding data, BOM defined, wafer testing.
  - Sample & production travellers for Assembly, Test and Qualification.

- **Commercial**
  - Die size estimates, unit cost re-estimate, fab timescales, any changes?

- **Quality, Reliability & Risk assessment.**
  - Quality plan review & update
  - Risks - review, any new risks identified?
From **DR3** to **DR4**

**DR3 Acceptance**
- GDSII Tape Out
  - Mask Making & Processing
    - Cut-'n-Go Prototype
    - Customer Evaluation
- Test Vectors
  - Test Specification
  - Test Program
    - Compliance Testing

**DR4 Acceptance**
Design Review 4

DR4

- Design
  - Specification, description, block diagrams & schematics etc.,
  - Samples meet specification, problems identified?

- Planning
  - Progress and outstanding actions.
  - Update of development plan, with production timescales.
  - Update of Production quantities & schedules.

- Manufacturing
  - Any problems/changes from Assembly, Test and Qualification?
  - Characterization data from samples.

- Commercial
  - Yield issues?

- Quality, Reliability.
  - Quality plan review & update
From **DR4 to DR5**

- **DR4 Prototype Acceptance**
  - Wafer Probe Test
  - Packaging
  - Final Delivery Test
  - Additional Process Tests & Yield Analysis
  - **DR5 Production Review**

*It Works*
Design Review 5

DR5

- Design
  - Yield issues, customer returns?

- Planning / Project
  - Outstanding actions.
  - Update of Production quantities & schedules.
  - Characterization / Qualification complete.

- Manufacturing
  - Any problems from Assembly, Test and Qualification?

- Commercial
  - Yield issues?

- Quality, Reliability.
  - Quality plan issued.

What Problems?

No Problems
Boss!
Some relevant considerations to getting it right!

Reliability
Risk Assessment
Packaging
Proving the design (verification)
Manufacturing
Commercial considerations
Reliability

• Application requirement
  – Operational life & Infant Mortality
  – Hazardous environment (to device)
  – Mission criticality?

• Environment
  – When device active?
  – Long term storage?
    • Operational and shelf storage

• Choice of Foundry
  – Appropriate technology?
  – Suitable design rules for application?
  – Characterised silicon for intended use?
Risk Assessment

• Chances of Success …
  – Avant-Garde design
  – Unusual techniques
  – Poor information
• Design criticality
• Failure Mode Analysis
• Life-Cycle requirements
  – Application
  – Environment
• Use of device outside of design rules
• Testability & Manufacturability
Packaging

- Ceramic / Plastic / Metal etc.,
- Package and lid match
  - number of pins
  - Electrical characteristics & performance
- Attach method ...
  - Eutectic
  - Ag-Glass
  - general Adhesives
- Bonding rules ...
  - Au or Al ?
  - Bond wire length and angles ?
  - Pad sizes and spacing
  - Current carrying capacity
- Lead finish
Design verification

Digital

- Verilog or VHDL netlists ...
  - Verilog often preferred by foundries
  - VHDL often preferred by Designers
- Pre- and Post-Layout checking ...
  - SDF file creation
  - Min-Typ-Max simulation
- Test benches
  - Fault coverage (stuck-at faults)
  - Automatic & Application Test Vector Generation
  - ATE Tester Vector Generation
  - ATE Tester semantics
  - Critical Path Timing data
- Test specification
  - Guardbanding
Design verification

Analog

• SPICE netlists ... 
  – Many SPICE flavours, netlist conversion?
• Pre- and Post-Layout checking ... 
  – Parasitic back extraction
  – Sweep & Monte Carlo simulation
• Test benches 
  – Multiple SPICE test benches
  – ATE Tester semantics
• Test specification 
  – Test set-up and parametric measurements critical.
  – Tester noise floor
  – Tester measurement resolution & accuracy
Design verification
Mixed Signal

• As both Analog & Digital, plus
• Signal / data-path partitioning
  – A/D & D/A interfacing techniques
  – Separate power/ground supplies?
• Test bench set-up now very critical ...
  – Mixed-mode simulation
  – Analog/Digital test synchronisation
• Testability
  – Intermediate test and capture points / nodes
  – Test equipment capability
  – Special test bench set-ups
• Test Specification !!!
  – Guardbanding
Manufacturing

• Test
  – Testability of design
    • adequate test coverage
  – Test socketing
    • Suitable for temperature extremes
  – Test throughput --- realistic tests
    • Test time vs. test coverage

• Manufacture
  – Acceptable yield profile
  – Special processing

• Project control
  – Project maintenance
  – Cost reduction
    • Test time reduction
    • Flow control
    • Volume purchasing
Commercial

• Projected yield
  – Gross Die / Wafer
  – Die yield at test
  – Yield after packaging

• Packaging costs

• Post processing ...
  – Device testing
  – Environmental screening
  – Life testing
Finally, the most important ingredients ...

Customer Involvement
Pragmatism
Honesty
ASE’s Design Capability

Software (CAD)
Hardware
Silicon vendor specific
ASE Design Tools

Software

• Cadence Tools (on Sun Sparc w/s)
  – Analog Artist Capture (Virtuoso Composer)
  – Analog Artist Layout (Virtuoso) with DLE
  – Spectre & cdsSpice
  – Verilog-XL
  – Verilog-Spectre Integration
  – DIVA Extraction
  – DIVA LVS, DRC and ERC

• Other
  – Tanner tools (LEDIT etc.,) pSpice
  – ECS capture system, Protel capture system
  – ModelSim (Mentor), with CodeRight
  – Actel Designer Software
ASE Design Tools

Hardware

• Design Hardware
  – Five Sun workstations (SunOS & Solaris)
  – Numerous PC’s (Win 9x, Win-XP, Win-7)
  – HP 36” colour plotter (Design Jet 1055CM)
  – Interfaces for
    • DAT
    • CDROM
    • QIC
    • ZIP
    • Floppy

• Hardware Archive
  – Rotating archive on DAT tape (incl. annual storage)
  – Nightly backup (every night)
ASE Design Tools

Vendor Kits

- Vendor kits installed include ...
  - Austria Micro Systems
  - X-Fab
  - Zetex (ASE Proprietary Cadence Kit)
  - Alcatel Mietec
  - Zarlink/MHS/Plessey Semiconductors
  - Chip Express (ASE Proprietary Cadence Kit)
  - MITEL
  - ACTEL
  - Others in various stages, such as
    - Micrel, VersArray, ES2, ABB-HAFO, SAMES, Atmel,
    - chartered Semi, Dynex, Prema, UTMC, Raytheon, Semefab,
    - Links to Europractice
In summary

• Design reviews are for ...
  – Customer partnership
  – Project & QA control
  – ultimate accuracy

These stringent controls have given us AND our customers 100% first time success in all ASIC projects!