# LINEAR SYSTEMS

### LSK389 ULTRA LOW NOISE MONOLITHIC DUAL N-CHANNEL JFET



## Linear Systems replaces discontinued Toshiba 2SK389 with LSK389

The 2SK389 / LSK389 is a monolithic matched dual JFET on a single chip

Why use On-Chip Dual JFET instead of 2 single JFETS?	FEATURES				
	ULTRA LOW NOISE	e <sub>n</sub> = 0.9nV/√Hz (typ)			
Save Cost	TIGHT MATCHING	V <sub>GS1-2</sub>   = 20mV max			
2SK389 / LSK389 removes significant cost for test screening time	HIGH BREAKDOWN VOLTAGE	BV <sub>GSS</sub> = 40V max			
needed to match lbss on 2 individual JFETS and offers ZERO yield loss.	HIGH GAIN	Y <sub>fs</sub> = 20mS (typ)			
	LOW CAPACITANCE 25pF ty				
	IMPROVED SECOND SOURCE REPLACEMENT FOR 2SK389				
Improve Performance	ABSOLUTE MAXIMUM RATINGS <sup>1</sup>				
2SK389 / LSK389 On-Chip lbss matching gives closest possible synchronous electrical performance and also offers better matched performance when the chip is subjected to temperature.	@ 25 °C (unless otherwise stated)				
	Maximum Temperatures				
	Storage Temperature	-65 to +150 °C			
	Operating Junction Temperature	-55 to +135 °C			
2SK389 / LSK389 Applications:	Maximum Power Dissipation				
End audio microphone, Audio Amplifier and audio effects box	Continuous Power Dissipation @ +125 °C	; 400mW			
Instrumentation-input stages of various instruments The acoustic sensor market –sonoboys / antisubmarine, military personnel and vehicle detectors, sonar makers. Radiation detectors.	Maximum Currents				
	Gate Forward Current $I_{G(F)} = 10$				
	Maximum Voltages				
	Gate to Source	$V_{GSS} = 40V$			
	Gate to Drain	$V_{GDS} = 40V$			

#### MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
$\left V_{GS1}-V_{GS2}\right $	Differential Gate to Source Cutoff Voltage			20	mV	$V_{DS}$ = 10V, $I_D$ = 1mA
IDSS1 IDSS2	Gate to Source Saturation Current Ratio	0.9			-	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V

### ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
$BV_{GSS}$	Gate to Source Breakdown Voltage		40			V	$V_{DS} = 0$ , $I_{D} = 100 \mu A$
$V_{\text{GS}(\text{OFF})}$	Gate to Source Pinch-off Voltage		0.15		2	V	$V_{DS}$ = 10V, $I_{D}$ = 0.1µA
	Drain to Source Saturation LS	LSK389A	2.6		6.5	mA	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0
I <sub>DSS</sub>		LSK389B	6		12		
		LSK389C	10		20		
I <sub>GSS</sub>	Gate to Source Leakage Current				200	pА	$V_{GS}$ = -30V, $V_{DS}$ = 0
Y <sub>fs</sub>	Full Conduction Transconductance		8	20		mS	$V_{DS}$ = 10V, $V_{GS}$ = 0, $I_{DSS}$ = 3mA, f = 1kHz
en	Noise Voltage			0.9	1.9	nV/√Hz	V <sub>DS</sub> = 10V, I <sub>D</sub> = 2mA, <i>f</i> = 1kHz, NBW = 1Hz
en	Noise Voltage			2.5	4	nV/√Hz	V <sub>DS</sub> = 10V, I <sub>D</sub> = 2mA, <i>f</i> = 10Hz, NBW = 1Hz
C <sub>ISS</sub>	Common Source Input Capacitance			25		pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, <i>f</i> = 1MHz,
C <sub>RSS</sub>	Common Source Reverse Transfer Cap.			5.5		pF	$V_{DG}$ = 10V, $I_{D}$ = 0, $f$ = 1MHz,

Available Packages: 2SK389 / LSK389 in SOIC-8 Lead 2SK389 / LSK389 in Thru-hole TO-71 6 Lead 2SK389 / LSK389 Toshiba footprint, SO8 / TO-71 with socket adaptor 2SK389 / LSK389 available as bare die 2SK389 / LSK389 available as wafer form Please contact Micross for package and die dimensions



